WHAT IS CLAIMED IS:

1. A method of forming a fin-shaped transistor, the method comprising:

providing a sacrificial fin structure in a compound semiconductor layer;

removing the sacrificial fin structure to form a trench in the compound semiconductor layer;

providing a fin-shaped strained silicon structure within the trench, the trench being associated with the fin-shaped transistor;

forming a gate structure for the fin-shaped strained silicon structure.

2. The method of claim 1, further comprising providing a sacrificial gate structure adjacent the sacrificial fin structure.

3. The method of claim 2, wherein the sacrificial gate structure includes nitride.

4. The method of claim 2, further comprising removing the sacrificial gate structure.

5. The method of claim 4, wherein the sacrificial gate structure includes polysilicon.

6. The method of claim 1, wherein the compound semiconductor layer includes a source region and a drain region, the sacrificial fin structure being between the source region and the drain region.

7. The method of claim 6, wherein the compound semiconductor layer is a silicon germanium layer.

8. The method of claim 6, wherein the sacrificial fin structure includes silicon germanium.

9. The method of claim 1, wherein the fin-shaped channel region has an aspect ratio of between approximately 1.5 and 3.0.

10. A method of forming a finFET, the method comprising:

providing a first layer above an insulating layer above a substrate, the first layer including silicon germanium, the first layer including a fin structure;

removing the fin structure to form an aperture in the first layer;

providing a strained material within the aperture; and

providing a gate structure for the strained material to form the finFET.

11. The method of claim 10, wherein the removing step is an etching step selective to the fin structure.

12. The method of claim 10, wherein the strained material is provided by selective silicon epitaxy.

13. The method of claim 10, further comprising forming a gate dielectric structure along sidewalls and a top of the strained material.

14. The method of claim 10, wherein the strained material is grown within the aperture in the first layer.

15. The method of claim 14, wherein strained material includes silicon.

16. The method of claim 15, wherein the fin structure is between a source region and a drain region.

17. A method of fabricating an integrated circuit including a fin-based transistor, the method comprising steps of:

providing an insulative material;

providing a strain-inducing layer above the insulative material, the strain-inducing layer including a narrow trench, the narrow trench including a sacrificial fin structure;

removing the sacrificial fin structure; and

forming a strained material in the narrow trench.

18. The method of claim 17, wherein the removing step is an etching step selective to the fin structure.

19. The method of claim 17, further comprising providing a gate structure for the strained material.

20. The method of claim 19, wherein the gate structure includes polysilicon.